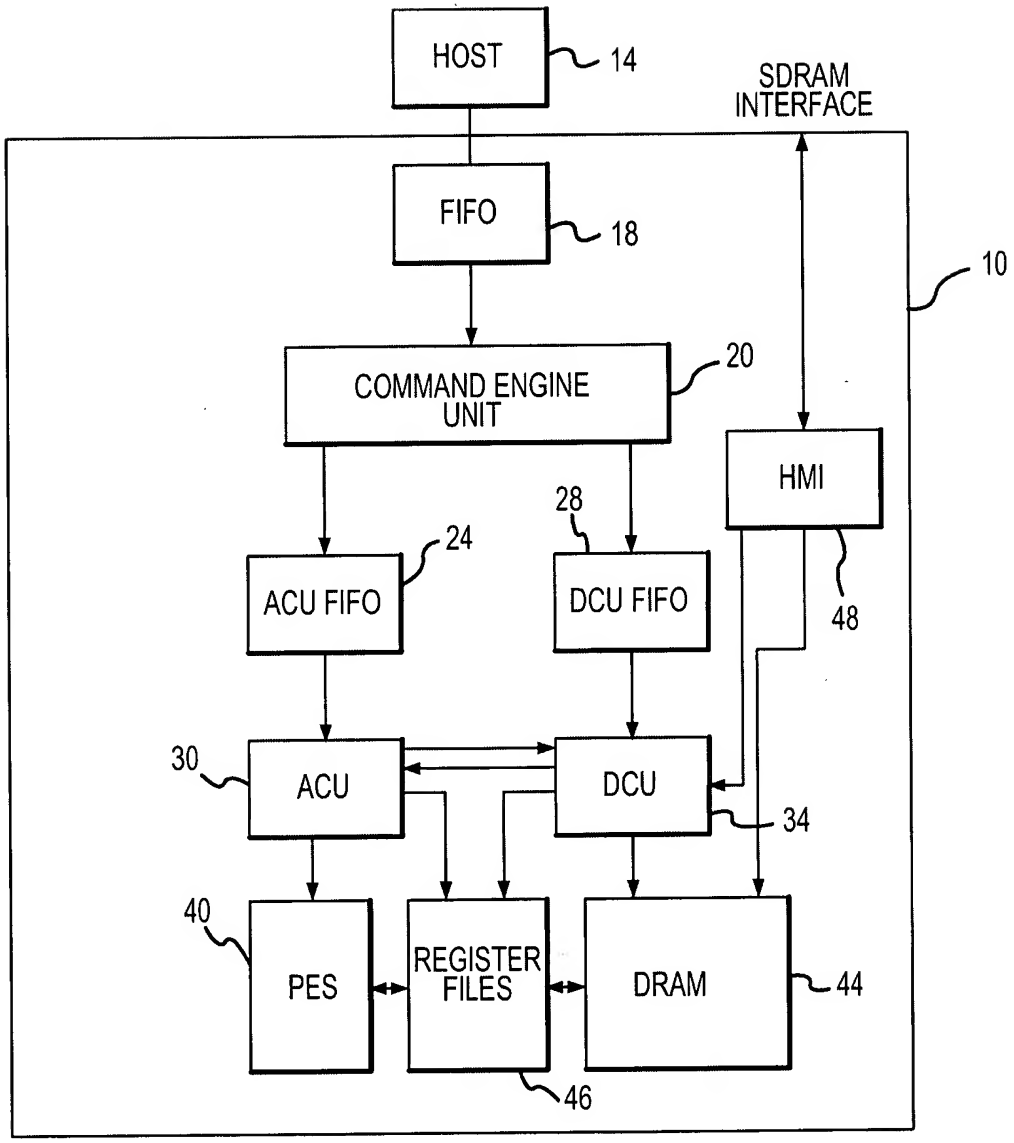
HOST
14
SDRAM
INTERFACE
FIFO
18
10
COMMAND ENGINE
UNIT
20
HMI
28
24
ACU FIFO
DCU FIFO
48
30
ACU
DCU
34
40
PES
REGISTER
FILES
DRAM
44
46

FIG.1

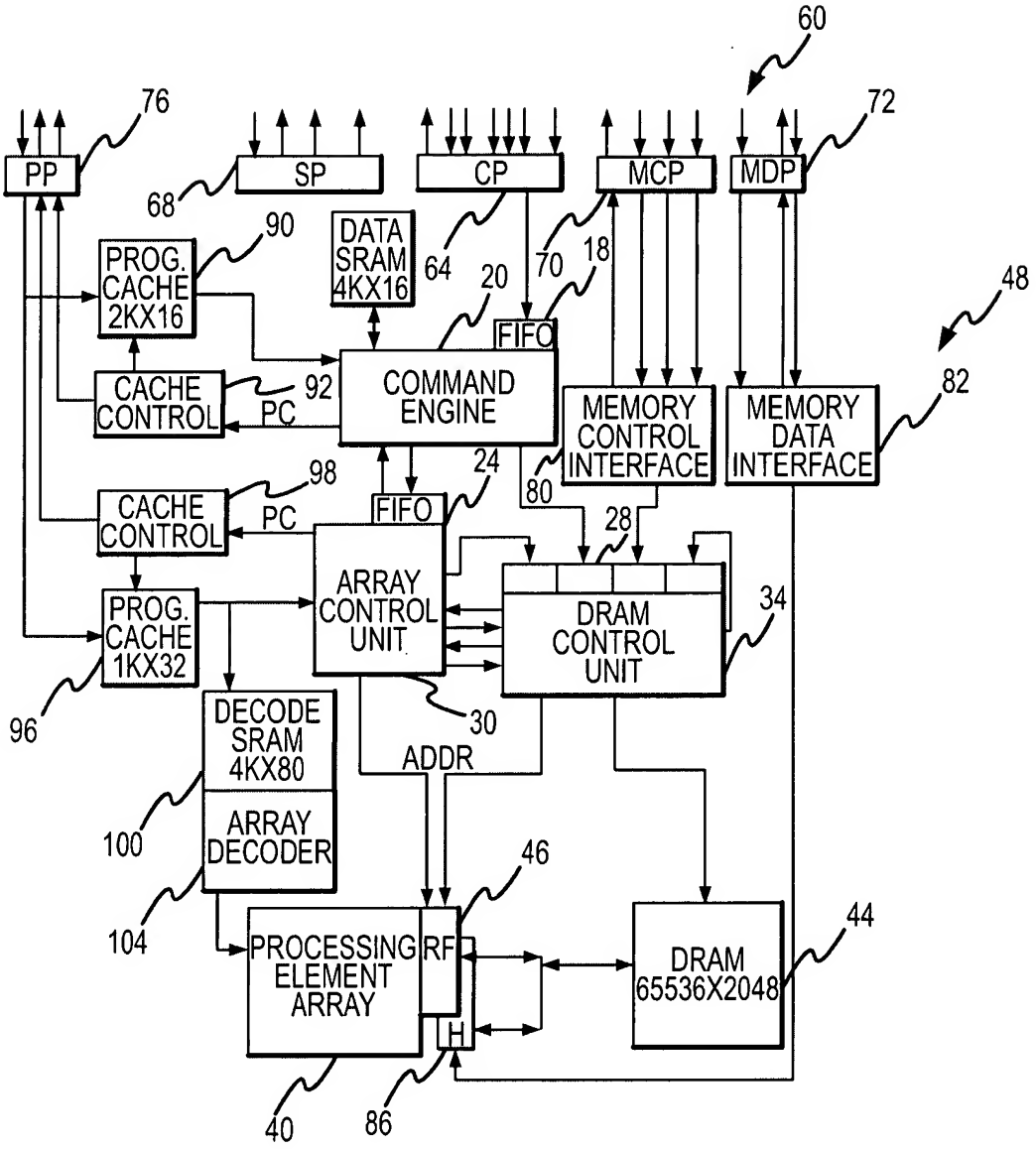
60
76
72
PP
SP
CP
MCP
MDP
68
64
70
18
48
90
DATA SRAM 4KX16
PROG. CACHE 2KX16
20
FIFO
CACHE CONTROL
92
PC
COMMAND ENGINE
MEMORY CONTROL INTERFACE
MEMORY DATA INTERFACE
82
98
24
80
CACHE CONTROL
PC
FIFO
28
ARRAY CONTROL UNIT
DRAM CONTROL UNIT
34
PROG. CACHE 1KX32
96
30
DECODE SRAM 4KX80
ADDR
100
ARRAY DECODER
46
104
PROCESSING ELEMENT ARRAY
RF
H
DRAM 65536X2048
44
40
86

FIG.2

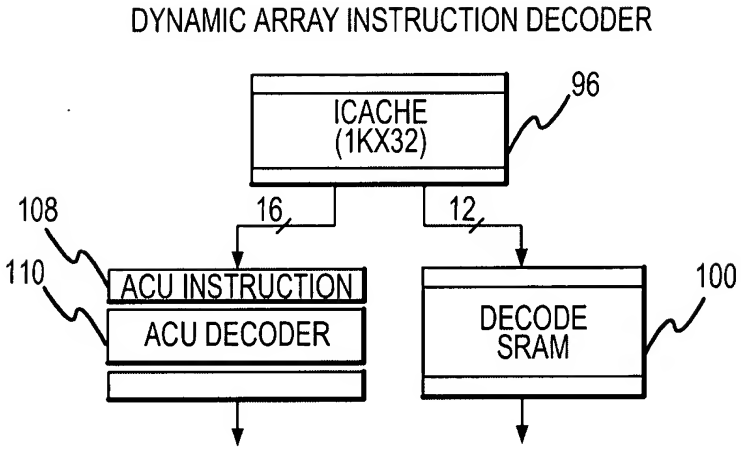
DYNAMIC ARRAY INSTRUCTION DECODER
ICACHE
(1KX32)
96
108
16
12
110
ACU INSTRUCTION
ACU DECODER
DECODE
SRAM
100

FIG.3

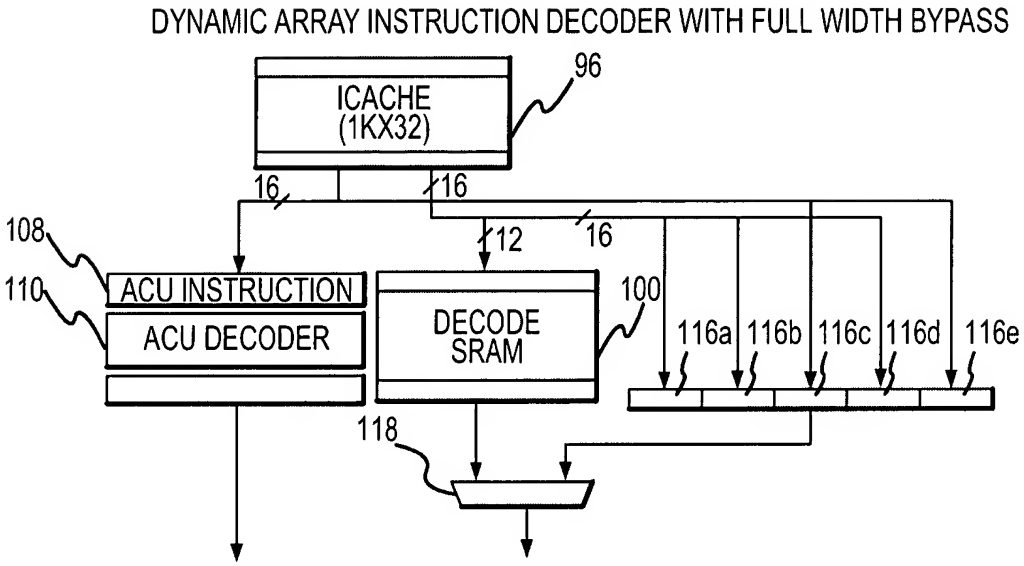
DYNAMIC ARRAY INSTRUCTION DECODER WITH FULL WIDTH BYPASS
ICACHE
(1KX32)
96
16
16
12
16
108
110
ACU INSTRUCTION
ACU DECODER
DECODE
SRAM
100
116a
116b
116c
116d
116e
118

FIG.4

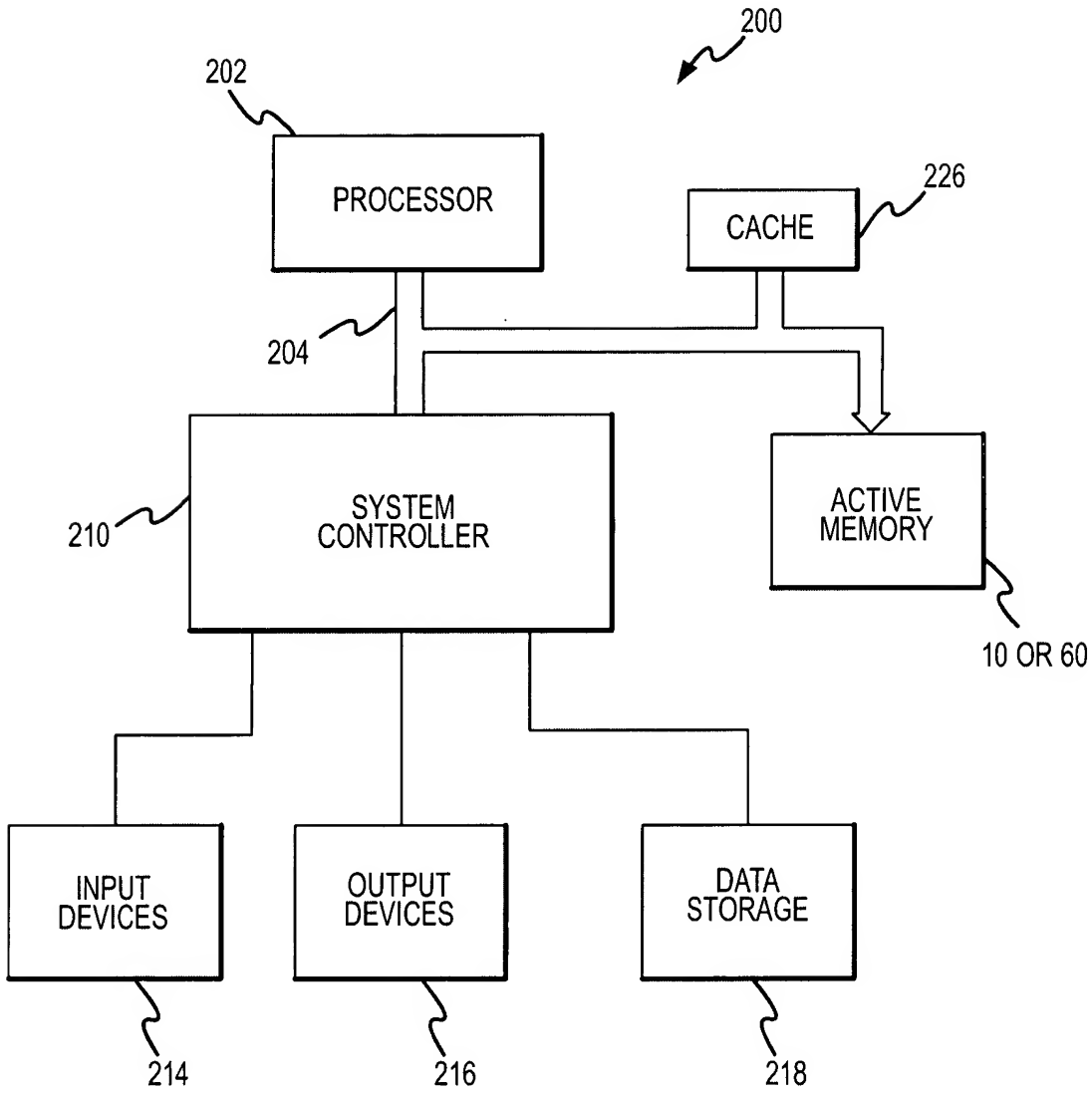
200
202
PROCESSOR
226
CACHE
204
210
SYSTEM CONTROLLER
ACTIVE MEMORY
10 OR 60
INPUT DEVICES
OUTPUT DEVICES
DATA STORAGE
214
216
218

FIG.5